

REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-21 are in the case. Claims 1, 5, 8, 12, 14, 17 and 20 have been amended.

Applicants acknowledge with appreciation the allowance of Claim 21.

Applicants also acknowledge with appreciation the indication of the allowability of Claims 5-9 and 12-17 if re-written in independent form and overcoming the informality objections. Applicants respectfully decline to re-write these claims in independent form at this time, in view of the reasons for the allowability of their base claims, set forth below, and respectfully request that for those reasons the objection to these claims for their dependency upon rejected base claims be reconsidered and withdrawn.

Regarding the objections to Claims 1-17 and 20, all of the suggestions to overcome the objections kindly provided by the Examiner have been made, with slight deviation regarding the suggested changes to Claim 12 that Applicants respectfully submit further improve form. It is therefore respectfully submitted that the objections have been overcome, wherefore their reconsideration and withdrawal are respectfully requested.

Regarding the rejection of Claims 1-4, 10, 11 and 18-20 under 35 U.S.C. §102(b) as allegedly being anticipated by Bayer, this rejection is respectfully traversed. Claims 1 and 18, the only independent claims subject to this rejection, both include a similar limitation, namely, in Claim 1 in pertinent part, the limitation "and discharge the output structure, *through the output interface*", and in Claim 18 in pertinent part, the limitation "the output structure is deactivated and discharges, *through the output interface*" (emphasis added). For example, in the embodiment shown in Figure 2, transistor 238 channels supplemental discharge current to load 246 by way of output 204, *and not into device 208*. As pointed out in the Specification at page 16, paragraph [0032],

lines 12-14, this reduces layout overhead and lowers power dissipation within device 208, improving design efficiency, cost and reliability.

The patent to Bayer apparently relates to an arrangement for driving a MOS FET, including a discharge circuit for discharging the gate-source capacitance of the driven FET according to a time constant. However, Bayer teaches a proposed solution that requires the current for this discharge to be channeled into his discharge circuit. Thus, referring to Bayer's Figure 3, when Bayer's control discharge signal S_E is applied to input E_E , transistors N1 and N2 turn on, conducting the current discharging C_{GS} into the ground M of the discharge circuit itself. Nor does Bayer suggest re-directing any of this discharge current to the load, through output terminal A. He is merely concerned with controlling switch-off time of his driven FET, while decreasing sensitivity to noise voltages, and is completely silent on reducing layout overhead or power dissipation, or improving design efficiency, cost or reliability. Thus, Bayer reveals no motivation to so re-direct his discharge current. The other art of record is even less relevant.

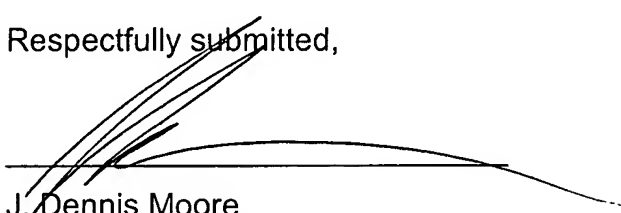
Therefore, it is respectfully submitted that for all of the above reasons Claims 1 and 18 are neither anticipated nor suggested by Bayer or, indeed, any of the art of record, whether considered individually or in any combination, and that therefore Claims 1 and 18 are allowable. Claims 2-4, 10, 11, 19 and 20 all depend, either directly or indirectly from on of Claims 1 and 18, and so are allowable as well for the same reasons, as well as for the additional limitations found therein. Wherefore reconsideration and withdrawal of this rejection are respectfully requested.

It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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